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TROUTMAN SANDERS LLP
600 PEACHTREE STREET , NE
ATLANTA, GA 30308

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,364	KREIFELS, JERRY A.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 as originally filed on 12/31/2003 are pending in the instant application. Of these, there are 3 independent claims and 17 dependent claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-16** are rejected under 35 U.S.C. 102(b) as being anticipated by Harari et al (US 5,369,615).

4. **Claim 1** is taught by Harari '615 as:

a. *An apparatus, comprising: a memory device including a block of memory operable to store data*. Figure 8a, discussed in column 15 lines 22-25, shows several sectors of a memory device

b. *Said memory device being adapted to at least partially erase said block of memory in a first erase cycle and in a second erase cycle subsequent to the first erase cycle*. Phase I erase and phase II erase of figure 7.

c. *Said memory device being further adapted to determine an erase performance for said block of memory during the first erase cycle.* Step 313 of figure 7, discussed in column 13 lines 36-38 show that the erasing is verified for the cells of Nref during phase I.

d. *Said memory device being further adapted to apply an erase pulse to said block of memory during the second erase cycle having an erase pulse voltage level based at least in part on the erase performance of said block of memory during the first erase cycle*. If the entire sector is not verified as erased in step 323 of figure 7, it VE is increased by dV in step 321 and the sector receives another erase pulse.

5. **Claim 2** is taught by Harari '615 as:

e. *The apparatus of claim 1, wherein the erase pulse comprises an initial erase pulse applied to said block of memory during the second erase cycle*. If a sector is not fully erased during Phase I, it receives another pulse when it begins Phase II.

6. **Claim 3** is taught by Harari '615 as:

f. *The apparatus of claim 2, wherein said memory device is further adapted to apply an initial erase pulse to said block of memory during the first erase cycle having an erase pulse voltage level.* The initial erase pulse is set to VE start in step 305 of figure 7, shown in column 12 line 31 to be the erase voltage of the first erase pulse.

g. *And wherein the erase pulse voltage level of the initial erase pulse applied to said block of memory during the second erase cycle is greater than the erase pulse voltage level of the initial erase pulse applied to said block of memory during the first erase cycle.* VE is increased in step 321 of figure 7, which is performed before the sector receives the first pulse of Phase II.

7. **Claim 4** is taught by Harari '615 as:

h. *The apparatus of claim 1, wherein the erase performance of said block of memory during the first erase cycle is based at least in part on the amount of time required to erase said block of memory.* Column 12 lines 46-50 show that the time of a pulse duration is constant in the disclosed invention. If the entire sector was not erased in the first pulse in phase I, erasing the sector has taken more than time t.

8. **Claim 5** is taught by Harari '615 as:

i. *The apparatus of claim 1, wherein said memory device is further adapted to apply a plurality of erase pulses to said block of memory during the first erase*

cycle and to count the number of erase pulses applied to said block of memory during the first erase cycle. While SDC is equal to 0, the sector remains in phase I. SDC is incremented until the sector passes the verification step 315. Accordingly, if the number of cells that fail the verification is higher than Nf, that cell remains in phase I. In step 316 VE is compared to VElimit to determine if VE is too high. As VE is incremented by dV in each cycle in step 321, the increase in VE represents the number of cycles during the first erase cycle.

j. *Said memory device being further adapted to determine the erase pulse voltage level of the erase pulse applied to said block of memory during the second erase cycle based at least in part on the number of erase pulses applied to said block of memory during the first erase cycle.* VE is increased during phase I by dV each time the sector is erased. Accordingly, when the sector enters phase II, VE is a function of how many erase pulses have been applied to the sector.

9. **Claim 6** is taught by Harari '615 as:

k. *The apparatus of claim 5, wherein said memory device is further adapted to compare the number of erase pulses applied to said block of memory during the first erase cycle to a threshold number of erase pulses.* In step 316 VE is compared to VE max. If VE has not been increased enough times to equal or exceed VEmax, the sector receives more erase pulses.

l. *And to change the erase pulse voltage level of the erase pulse applied to said block of memory during the second erase cycle if the number of erase pulses applied to said block of memory during the first erase cycle is not less than the threshold number of erase pulses.* If VE has been increased enough times to exceed VEmax, the sector is mapped as a bad sector and removed from erase processing. Accordingly, mapping the sector as bad and untagging the sector, the erase pulse voltage level of the erase pulse applied to the sector is set to no voltage.

10. **Claim 7** is taught by Harari '615 as:

m. *The apparatus of claim 1, wherein said memory device further includes a memory location adapted to store the erase pulse voltage level of the erase pulse, and wherein said memory device is further adapted to store the erase pulse voltage level of the erase pulse in said memory location.* Column 15 lines 22-25 show that the VEstart is stored in item 361 for each sector. Column 15 lines 29-34 show that the VE required when phase I is completed is stored in the memory when the algorithm proceeds to phase II.

11. **Claim 8** is taught by Harari '615 as:

n. *The apparatus of claim 7, wherein said block of memory comprises a first block of memory and said memory location comprises a first memory location*

uniquely associated with said first block of memory. Column 15 lines 22-25 show that the VE start is stored for each sector.

o. *Wherein said memory device further comprises a second block of memory and a second memory location uniquely associated with said second block of memory*. Figure 8a shows multiple sectors 263, each having an associated VEstart 361.

p. *And wherein said second memory location is adapted to store an erase pulse voltage level associated with an erase pulse applied to said second block of memory*. Figure 8a shows multiple sectors 263, each having an associated VEstart 361.

12. **Claim 9** is taught by Harari '615 as:

q. *A method, comprising: determining the erase performance of a block of memory of a memory device during a first erase cycle of the block of memory.* Steps 313 and 315 of figure 7, discussed in column 13 lines 336-42, show that the number of cells that are erased out of Nref are sufficient to go directly to the verification of all the cells of the sector.

r. *And using the determined erase performance to optionally set the erase pulse voltage level of an erase pulse applied to the block of memory during a second erase cycle subsequent to the first erase cycle*. In step 316 If VE is less than VElimit the algorithm goes to step 317, and once all sectors have received the first erase pulse, VE is incremented in step 321 is there are unerased

sectors. If VE not less than VElimit, the sector is mapped out as a bad sector, column 13 lines 43-48.

13. **Claim 10** is taught by Harari '615 as:

s. *The method of claim 9, wherein determining the erase performance of the block of memory comprises monitoring the amount of time required to erase the block of memory during the first erase cycle*. Column 12 lines 46-50 show that the time of a pulse duration is constant in the disclosed invention. If the entire sector was not erased in the first pulse in phase I, erasing the sector has taken more than time t.

14. **Claim 11** is taught by Harari '615 as:

t. *The method of claim 9, wherein determining the erase performance of the block of memory comprises counting a total number of erase pulses applied to the block of memory during the first erase cycle*.

15. **Claim 12** is taught by Harari '615 as:

u. *The method of claim 11, wherein using the determined erase performance to optionally set the erase pulse voltage level comprises comparing the total number of erase pulses to a threshold number of erase pulses, and setting the erase pulse voltage level of the erase pulse if the total number of erase pulses is not less than the threshold number of erase pulses.*

16. **Claim 13** is taught by Harari '615 as:

v. *The method of claim 9, wherein the erase pulse voltage level comprises an initial erase pulse voltage level.* Column 12 lines 31-40 show that VEstart is the erase voltage of the first pulse.

17. **Claim 14** is taught by Harari '615 as:

w. *The method of claim 9, wherein the method further comprises, if the erase pulse voltage level is set, storing the erase pulse voltage level of the erase pulse in a memory location uniquely associated with the block of memory.* Column 15 lines 29-34 show that the set VE value for the sector is stored as the updated VEstart 361 for the sector.

18. **Claim 15** is taught by Harari '615 as:

x. *The method of claim 9, wherein the block of memory is a first block of memory and the method further comprises: determining the erase performance of a second block of memory of the memory device during a first erase cycle of the second block of memory.* When a second sector is to be erased, it enters Phase I after the first sector finishes Phase I, as shown by figure 7.

y. *And using the determined erase performance to optionally set the erase pulse voltage level of an erase pulse applied to the second block of memory during a second erase cycle subsequent to the first erase cycle.* Figure 7 shows

that if all sectors are not untagged, *i.e.* not fully erased, VE is increased in step 321.

19. **Claim 16** is taught by Harari '615 as:

z. *The method of claim 15, wherein the method further comprises, if the erase pulse voltage level of an erase pulse applied to the second block of memory is set, storing the erase pulse voltage level of the erase pulse applied to the second block of memory in a memory location uniquely associated with the second block of memory.* Column 15 lines 29-34 show that as soon as the cells Nref of a sector are properly verified, the VE value for that stage is stored as the updated VEstart for that sector.

20. **Claims 1-7, 9-13, and 15** are rejected under 35 U.S.C. 102(e) as being anticipated by Bautista et al. (US 6,891,752).

21. **Claim 1** is taught by Bautista as:

aa. *An apparatus, comprising: a memory device including a block of memory operable to store data.* Column 5 lines 10-13 show that the disclosed invention is directed toward erase voltage control during multiple sector erase of a flash memory device.

bb. *Said memory device being adapted to at least partially erase said block of memory in a first erase cycle and in a second erase cycle subsequent to the first*

erase cycle. Column 10 lines 4-7 show that an erase pulse is applied to the four sectors, a block of memory in the memory device, selected to be erased. Column 10 lines 12-14 show that after verifying that the first memory sector is erased, the second sector is verified. If the second sector is not erased an erase pulse is applied to the second and fourth memory sectors.

cc. *Said memory device being further adapted to determine an erase performance for said block of memory during the first erase cycle*. Column 8 line 65 through column 9 line 1 discusses the verification step (item 720 of figure 7A), during which the performance of the erase pulse is checked.

dd. *Said memory device being further adapted to apply an erase pulse to said block of memory during the second erase cycle having an erase pulse voltage level based at least in part on the erase performance of said block of memory during the first erase cycle*. If the verification step determined that the sector was not erased, the erase pulse voltage is increased (Column 8 line 65 through column 9 line 1). Column 9 lines 31-33 show that the gate erase voltage is only reset upon selection of another block of memory to erase. This is shown by item 975 of figure 9 to occur after multiple erase cycles, items 920, 940, 950, and 965, have been performed. Accordingly, the erase voltage is increased during the first erase cycle, and remains increased during the second erase cycle.

22. **Claim 2** is taught by Bautista as:

ee. *The apparatus of claim 1, wherein the erase pulse comprises an initial erase pulse applied to said block of memory during the second erase cycle.* Column 10 lines 12-14 shows that an erase pulse is applied at step 935, which part of the second erase cycle.

23. **Claim 3** is taught by Bautista as:

ff. *The apparatus of claim 2, wherein said memory device is further adapted to apply an initial erase pulse to said block of memory during the first erase cycle having an erase pulse voltage level.* Column 9 lines 37-38 shows that when the group of sectors is selected for erase, the gate erase voltage is set to an initial value.

gg. *And wherein the erase pulse voltage level of the initial erase pulse applied to said block of memory during the second erase cycle is greater than the erase pulse voltage level of the initial erase pulse applied to said block of memory during the first erase cycle.* Column 10 lines 8-10 shows that the gate erase voltage is increased until the first memory sector is verified as erased. As the gate erase voltage is only reset when a new group of unerased sectors is selected, the initial erase pulse applied during the second cycle is higher than the initial pulse of the first erase cycle.

24. **Claim 4** is taught by Bautista as:

hh. *The apparatus of claim 1, wherein the erase performance of said block of memory during the first erase cycle is based at least in part on the amount of time required to erase said block of memory*. Column 3 lines 21-22 show that an erase pulse is a voltage applied for a period of time. Column 3 lines 40-41 show that extra pulses result in longer erase times. Accordingly, the number of pulses needed to erase a block of memory determines the amount of time needed to erase the memory. Column 10 lines 8-10 show that the erase voltage may be increased after a number of pulses have been applied, which is an amount of time required to erase the sector.

25. **Claim 5** is taught by Bautista as:

ii. *The apparatus of claim 1, wherein said memory device is further adapted to apply a plurality of erase pulses to said block of memory during the first erase cycle and to count the number of erase pulses applied to said block of memory during the first erase cycle*. Column 9 lines 51-53 shows that the voltage can be adjusted after four pulses have been applied. In order to know that four pulses have been applied, it is inherent that the number of erase pulses applied to the block of memory are counted.

jj. *Said memory device being further adapted to determine the erase pulse voltage level of the erase pulse applied to said block of memory during the second erase cycle based at least in part on the number of erase pulses applied to said block of memory during the first erase cycle*. Column 9 lines 31-33 shows

that the gate erase voltage is only reset when another group of unerased sectors is selected. Figure 9 item 975 shows that the gate voltage is not reset until after all of the selected sectors have been erased, which is after the first erase cycle, items 915, 920 and 925, and the second erase cycle, 930, 935, and 940.

26. **Claim 6** is taught by Bautista as:

kk. *The apparatus of claim 5, wherein said memory device is further adapted to compare the number of erase pulses applied to said block of memory during the first erase cycle to a threshold number of erase pulses.* Column 9 lines 51-53 shows that the voltage can be adjusted after four pulses have been applied. Accordingly, four pulses is a threshold in this example.

ll. *And to change the erase pulse voltage level of the erase pulse applied to said block of memory during the second erase cycle if the number of erase pulses applied to said block of memory during the first erase cycle is not less than the threshold number of erase pulses.* As shown in column 9 lines 51-53, the gate voltage can be changed after four pulses, which is not less than the threshold number of erase pulses. The gate voltage applied during the first erase cycle is the same as the gate voltage applied during the second erase cycle, column 9 lines 31-33.

27. **Claim 7** is taught by Bautista as:

mm. *The apparatus of claim 1, wherein said memory device further includes a memory location adapted to store the erase pulse voltage level of the erase pulse, and wherein said memory device is further adapted to store the erase pulse voltage level of the erase pulse in said memory location.* Column 10 lines 43-45 show that the processes shown in figures 8 and 9 can be embedded in the logic of the state control and command register control. As the gate voltage is increased during the process shown in figure 9, and the increased voltage is remembered during the steps of erasing, column 9 lines 23-33, and is reset when the selected sectors are verified to be erased, column 9 lines 31-33, figure 9 step 975, it is inherent that the voltage level of the erase pulse is stored in a memory location, as otherwise the system would be unable to remember the changed erase pulse voltage level and unable to reset the erase pulse voltage level.

28. **Claim 9** is taught by Bautista as:

nn. *A method, comprising: determining the erase performance of a block of memory of a memory device during a first erase cycle of the block of memory.* Column 8 line 65 through column 9 line 1 discusses the verification step (item 720 of figure 7A), during which the performance of the erase pulse is checked.

oo. *And using the determined erase performance to optionally set the erase pulse voltage level of an erase pulse applied to the block of memory during a second erase cycle subsequent to the first erase cycle.* If the verification step determined that the sector was not erased, the erase pulse voltage is increased

(Column 8 line 65 through column 9 line 1). Column 9 lines 31-33 show that the gate erase voltage is only reset upon selection of another block of memory to erase. This is shown by item 975 of figure 9 to occur after multiple erase cycles, items 920, 940, 950, and 965, have been performed. If the set of memory cells are verified to be erased, the erase voltage is not increased.

29. **Claim 10** is taught by Bautista as:

pp. *The method of claim 9, wherein determining the erase performance of the block of memory comprises monitoring the amount of time required to erase the block of memory during the first erase cycle.* Column 3 lines 21-22 show that an erase pulse is a voltage applied for a period of time. Column 3 lines 40-41 show that extra pulses result in longer erase times. Accordingly, the number of pulses needed to erase a block of memory determines the amount of time needed to erase the memory. Column 10 lines 8-10 show that the erase voltage may be increased after a number of pulses have been applied, which is an amount of time required to erase the sector. By monitoring the number of pulses, the time required to erase the memory is monitored.

30. **Claim 11** is taught by Bautista as:

qq. *The method of claim 9, wherein determining the erase performance of the block of memory comprises counting a total number of erase pulses applied to the block of memory during the first erase cycle.* Column 9 lines 51-53 shows

that the voltage can be adjusted after four pulses have been applied. In order to know that four pulses have been applied, it is inherent that the number of erase pulses applied to the block of memory are counted.

31. **Claim 12** is taught by Bautista as:

rr. *The method of claim 11, wherein using the determined erase performance to optionally set the erase pulse voltage level comprises comparing the total number of erase pulses to a threshold number of erase pulses, and setting the erase pulse voltage level of the erase pulse if the total number of erase pulses is not less than the threshold number of erase pulses.* As shown in column 9 lines 51-53, the gate voltage is changed after four pulses, which is not less than the threshold number of erase pulses. The gate voltage applied during the first erase cycle is the same as the gate voltage applied during the second erase cycle, column 9 lines 31-33.

32. **Claim 13** is taught by Bautista as:

ss. *The method of claim 9, wherein the erase pulse voltage level comprises an initial erase pulse voltage level.* Column 9 lines 38-39 show that the gate erase voltage is set to an initial value.

33. **Claim 15** is taught by Bautista as:

tt. *The method of claim 9, wherein the block of memory is a first block of memory and the method further comprises: determining the erase performance of a second block of memory of the memory device during a first erase cycle of the second block of memory*. Column 3 lines 56-59 shows that a subset of sectors is selected to be erased, which forms the first block of memory. Selecting a second block subset of sectors forms the second block of memory. Item 980 of figure 9, discussed at column 10 lines 37-40, shows that if there is a subset of sectors that is left to be erased, the second block of memory, the process shown in figure 9 is repeated for the sectors of memory to be erased.

uu. *And using the determined erase performance to optionally set the erase pulse voltage level of an erase pulse applied to the second block of memory during a second erase cycle subsequent to the first erase cycle*. If the verification step determined that the sector was not erased, the erase pulse voltage is increased (Column 8 line 65 through column 9 line 1). Column 9 lines 31-33 show that the gate erase voltage is only reset upon selection of another block of memory to erase. This is shown by item 975 of figure 9 to occur after multiple erase cycles, items 920, 940, 950, and 965, have been performed. If the set of memory cells are verified to be erased, the erase voltage is not increased.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. **Claims 17-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al (US 5,369,615) in view of Harari et al. (US 5,297,148).

36. **Claim 17** is taught by Harari '615 as:

vv. *An apparatus, comprising: a first block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle.* See column 12 lines 51-55, which show phase I and phase II. Fig 7 shows that Phase II occurs after phase I.

ww. *A first memory location uniquely associated with said first block of memory, said first memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle.* Column 15 lines 22-25 show that the VEstart, the initial erase voltage, is stored for each sector.

xx. *A second block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle.* Figure 8a, discussed in column 15 lines 22-25 show that there are multiple sectors in the memory device.

yy. *A second memory location uniquely associated with said second block of memory, said second memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle.* Item 361 of figure 8a shows that VEstart, the initial erase pulse voltage level, is stored for each sector.

zz. *And, a processing unit adapted to evaluate erase performance of said first block of memory during the first erase cycle therefor and to evaluate erase performance of said second block of memory during the first erase cycle therefor.* Step 315 of figure 7, discussed in column 13 lines 39-42, involves checking the erasure of cells performed in phase I, which is an evaluation of the erase cycle.

aaa. *Said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said first block of memory based at least in part on the evaluated erase performance of said first block of memory.* Column 15 lines 29-34 show that the VE value generated at the end of phase I is stored as the updated VEstart for that sector.

bbb. *And said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said second block of memory based at least in part on the evaluated erase performance of said second block of memory.* Column 15 lines 29-34 show that the VE value generated at the end of phase I is stored as the updated VEstart for that sector.

37. Harari '615 does not expressly teach that the evaluation of erase performance and the storing of erase pulse voltage level for the first and second memory blocks are performed by a processing unit.

38. Harari '148 teaches the use of a controller to perform erase operations (column 5 lines 34-36, and to perform verification on erased sectors (column 6 lines 52-54).

39. Harari '615 and Harari '148 are analogous art because they are from the same field of endeavor, EEPROM memory devices and methods for use in EEPROM memory devices.

40. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a controller as shown by Harari '148 to perform the erasing method of Harari '615.

41. The motivation for doing so would have been that Harari '615 incorporates US patent Application 337,566, of which Harari '148 is a division, in column 6 lines 58-62as a teaching of methods and a device for multiple sector erase of a flash memory. Further motivation comes from the knowledge of one of ordinary skill in the art that in order to implement a method such as that shown in figure 7 of Harari '615, a controller is necessary. Further motivation comes from Harari '148 column 1 line 65 to column 2 line 3, which shows that the invention disclosed allows any combination of sectors among the chips to be selected and erased simultaneously, which is faster and more efficient than prior art schemes.

42. Therefore it would have been obvious to combine Harari '148 with Harari '615 for the benefit of having a device to perform the erase algorithm of Harari '615 to obtain the invention as specified in **claims 17-20**.

43. **Claim 18** is taught by Harari '615 as:

ccc. *The apparatus of claim 17, wherein the initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle thereof is different than the initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle thereof.* Column 15 lines 47-50 shows that the two-phase erase algorithm is applicable to memory arrays having sectors with different optimum erase voltages. Column 15 lines 29-34 shows that the VE value generated at the end of phase I is stored as the updated VEstart for that sector, and each sector is shown in figure 8a to have a corresponding VEstart, item 361.

44. **Claim 19** is taught by Harari '148 as:

ddd. *The apparatus of claim 17, wherein said apparatus further comprises a voltage source operable to apply erase pulses having respective desired erase pulse voltage levels to said first block of memory and to said second block of memory in response to signals received from said processing unit.* Erase Voltage 209 of figure 3a is shown in column 5 lines 63-68 to be issued by the controller to erase all the selected sectors.

45. **Claim 20** is taught by Harari '615 as:

eee. *The apparatus of claim 17, wherein said processing unit is further adapted to count erase pulses applied to said first block of memory during the first erase cycle thereof in order to evaluate erase performance of said first block of memory*. SDC is incremented at each cycle, column 14 lines 4-6.

fff. *And to compare the count to a threshold value in order to determine whether to increase the initial erase pulse voltage for an erase pulse to be applied to said first block of memory during the second erase cycle thereof.* Step 321 of figure 7, discussed in column 13 lines 57-59 shows that VE is incremented by dV, a constant. In step 331 of figure 7, discussed in column 14 lines 7-15, it is checked if VE has exceeded VE limit or if SDC has exceeded Nmax, which creates upper limits on the number of pulsing and verification cycles.

ggg. *And wherein said processing unit is further adapted to count erase pulses applied to said second block of memory during the first erase cycle thereof in order to evaluate erase performance of said second block of memory*. Step 331 is performed for each sector to be erased.

hhh. *And to compare the count to a threshold value in order to determine whether to increase the initial erase pulse voltage for an erase pulse to be applied to said second block of memory during the second erase cycle thereof.* Step 331 is performed for each sector to be erased.

Conclusion

46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

47. Miyakawa et al. (US 5,920,508) teaches a method of erasing non-volatile memory involving three cycles.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Jared I Rutz
Examiner
Art Unit 2187

jir

DONALD SPARKS
SUPERVISORY PATENT EXAMINER